[Abstract of the Disclosure]

[Abstract]

A ferroelectric memory device and methods of the same are provided, in which one extended plate line is directly contact with ferroelectric capacitors arranged on at least two adjacent rows in a cell array area. Alternatively, the ferroelectric capacitors on the at least tow adjacent rows share one common top electrode, which is directly contact with the extended plate line. The plate line is composed of a local plate line and a main plate line or only one of them. The local plate line is formed by the steps of forming a plurality of ferroelectric capacitors in the cell array area, forming a bottom plate layer thereon, and patterning the bottom plate layer. The main plate line is formed by the steps of forming an upper interlayer dielectric on an entire surface of the semiconductor substrate having the plurality of the ferroelectric capacitors or the local plate line, patterning the upper interlayer dielectric to form a slit-type via hole, forming an top plate layer covering the slit-type via hole, and patterning the top plate layer.

[Typical Figure]

Fig. 5

[Specification]

[Title of the Invention]

FERROELECTRIC MEMORY DEVICE HAVING EXPANDED PLATE LINES AND METHOD OF FABRICAING THE SAME

[Brief Description of Drawings]

Fig. 1 through Fig. 3 are cross-sectional views for explaining a method of fabricating a ferroelectric memory device according to a prior art.

Fig. 4 is a top plan view showing a cell array area of a ferroelectric memory device according to the present invention.

Fig. 5 is a perspective view for explaining a ferroelectric memory device according to one embodiment of the present invention.

Fig. 6 is a perspective view for explaining a ferroelectric memory device according to another embodiment of the present invention.

Fig. 7 is a perspective view for explaining a ferroelectric memory device according to still another embodiment of the present invention.

Fig. 8 through Fig. 14 are cross-sectional views for explaining a method of fabricating a ferroelectric memory device according to one embodiment of the present invention, taken along a line I-I' of Fig. 4.

Fig. 15 through Fig. 19 are cross-sectional views for explaining a method of fabricating a ferroelectric memory device according to another embodiment of the present invention, taken along a line I-I' of Fig. 4.

Fig. 20 through Fig. 24 are cross-sectional views for explaining a method of fabricating a ferroelectric memory device according to still another embodiment of the present invention, taken along a line I-I' of Fig. 4.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention generally relates to a semiconductor device and a method of fabricating the same. More specifically, the present invention is directed to a ferroelectric memory device having expanded plate lines and a method of fabricating the same.

Ferroelectric memory devices continuously hold their stored data even when their power supplies are interrupted. Further, ferroelectric memory devices operate at a low power supply voltage, which is similar to DRAM and SRAM. As a result, ferroelectric devices are attractive as candidates for smart cards or the like.

A conventional method of fabricating a ferroelectric memory device will be described with reference to Fig. 1 through Fig. 3.

Referring now to Fig. 1, device isolation layers 13 are formed in predetermined areas of a semiconductor substrate 11 to define active regions. A plurality of insulated gate electrodes 15, i.e., wordlines are formed to cross over the active regions and the device isolation layers 13. Thereafter,

impurities are implanted into the active region between the gate electrodes 15 to form source/drain regions 17s and 17d. A first lower interlayer dielectric 19 is formed on an entire surface of the resultant structure in which the source/drain regions 17s and 17d are formed. The first lower interlayer dielectric 19 is patterned to form storage node contact holes that expose the source regions 17s. Contact plugs 21 are then formed in the storage node contact holes.

Referring to Fig. 2, ferroelectric capacitors 32 are 2-dimensionally arranged on an entire surface of a semiconductor substrate having the contact plugs 21. Each of the ferroelectric capacitors 32 is composed of a bottom electrode 27, a ferroelectric layer pattern 29, and a top electrode 31 which are sequentially stacked. Each of the bottom electrodes 27 covers the contact plug 21. A first upper interlayer dielectric 33 is formed on an entire surface of the semiconductor substrate having the ferroelectric capacitors 32. A plurality of main wordlines 35, which are parallel with the gate electrodes 15, are then formed on the first upper interlayer dielectric 33. Each of the main wordlines 35 generally controls four wordlines 15.

Referring now to Fig. 3, a second upper interlayer dielectric 37 is formed on an entire surface of the semiconductor substrate having the main wordlines 35. The second and first interlayer dielectrics 37 and 33 are patterned to form via holes 39 that expose the top electrodes 31. To reduce an aspect ratio of each of the via holes 39, wet and dry etch technique can be applied. In this case, the via hole 39 has an inclined upper sidewall 39a, as shown in Fig. 3. Unfortunately, excessive wet-etch results in exposure of the main wordline 35.

As another approach to reduce an aspect ratio of the via hole 39, a diameter of the via hole 39 can be increased. However, a spacing (s) between the via hole 39 and an adjacent main wordline 35 gradually decreases with increase in integration level of ferroelectric memory devices. This makes requisition for precise alignment during a photo process for forming the via hole 39.

Continuously, a plurality of plate lines 41 are formed to cover the via holes 39. The plate lines 41 are arranged to be parallel with the wordlines 35.

According to the foregoing prior art, decreasing an aspect ratio of the via holes leads to a strong probability that the main wordlines will be exposed. Therefore, it is hard to avoid an electric short between the plate line and the main wordline as well as a contact failure between the top electrode and the plate line.

[Technical Object of the Invention]

It is an object of the present invention to provide a ferroelectric memory device which can maximize a contact area between a plate line and a top electrode, and securing an insulation characteristic between the plate line and a main wordline.

It is another object of the present invention to provide a method of fabricating a ferroelectric memory device which can maximize a contact area between a plate line and a top electrode, and securing an insulation characteristic between the plate line and a main wordline.

[Construction of the Invention]

According to one aspect of the present invention, there is provided a ferroelectric memory device having expanded plate lines that are in directly contact with top electrodes arranged on at least two adjacent rows. The ferroelectric memory device includes a lower interlayer dielectric formed on a semiconductor substrate. A plurality of ferroelectric capacitors are 2-dimensionally arranged on the lower interlayer dielectric along rows and columns. An upper interlayer dielectric covers an entire surface of the semiconductor substrate having the ferroelectric capacitors. The upper interlayer dielectric consists of first and second upper interlayer dielectrics that are sequentially stacked. A plurality of plate lines are arranged in the upper interlayer dielectric in parallel with the column direction. Each of the plate lines is directly contact with upper surfaces of the ferroelectric capacitors that are arranged on the at least two adjacent rows. As a result, the ferroelectric capacitors arranged on at least adjacent two rows share one plate line. In addition, a plurality of main wordlines can be arranged between the first and second upper interlayer dielectrics in parallel with the column direction.

The plate line is a local plate line covered with the upper interlayer dielectric or a main plate line covering a slit-type via hole that is formed through the upper interlayer dielectric. Alternatively, the plate line may include the local plate line and the main plate line. Each of the slit-type via holes is located between the main wordlines.

Each of the ferroelectric capacitors comprises a bottom electrode, a ferroelectric layer pattern, and a top electrode that are sequentially stacked. In this case, each of the plate lines is directly contact with the top electrodes

that are arranged on at least two adjacent rows. Preferably, a gap area between the ferroelectric capacitors is filled with a material layer having an etch selectivity with respect to the upper interlayer dielectric.

Furthermore, each of the ferroelectric capacitors may comprises a bottom electrode, a ferroelectric layer pattern, and a common top electrode that are sequentially stacked. The common top electrode covers the ferroelectric layer patterns that are arranged on the at least two adjacent rows. Preferably, gap areas between the bottom electrodes and between the ferroelectric layer patterns are filled with an insulating pattern. As a result, the ferroelectric capacitors arranged on the at least two adjacent rows share one common top electrode. In this case, the common top electrode is directly contact with the plate line.

Furthermore, each of the ferroelectric capacitors may comprises a bottom electrode, a common ferroelectric layer pattern, and a common top electrode that are sequentially stacked. The common ferroelectric layer pattern covers the bottom electrodes that are arranged on the at least two adjacent rows. The common ferroelectric layer pattern and the common top electrode overlap with each other. Accordingly, the common top electrode is directly contact with the plate line.

According to another aspect of the present invention, there is provided a method of fabricating a ferroelectric memory device having expanded plate lines that are directly contact with top electrodes arranged on at least two adjacent rows. In this method, a lower interlayer dielectric is formed on a semiconductor substrate. A plurality of ferroelectric capacitors are 2-dimensionally arranged on the lower interlayer dielectric along rows

and columns. An upper interlayer dielectric and a plurality of plate lines arranged therein are formed on an entire surface of the semiconductor substrate having the ferroelectric capacitors. The plate lines are parallel with the column direction. Each of the plate lines is directly contact with upper surfaces of the ferroelectric capacitors that are arranged on the at least two adjacent rows. The upper interlayer dielectric can be formed by sequentially stacking first and second upper interlayer dielectric.

A method of fabricating the ferroelectric capacitors includes the steps of sequentially forming a bottom electrode layer, a ferroelectric layer, and a top electrode layer on the lower interlayer dielectric, and successively patterning the top electrode layer, the ferroelectric layer, and the bottom electrode layer. Thus, each of the ferroelectric capacitors comprises a bottom electrode, a ferroelectric layer pattern, and a top electrode that are sequentially stacked. In this case, each of the plate lines is contact with the top electrodes that are arranged on the at least two adjacent rows. Preferably, an insulating pattern is formed to fill a gap area between the ferroelectric capacitors.

Alternatively, a method of fabricating the plurality of ferroelectric capacitors includes a step of sequentially forming a bottom electrode layer and a ferroelectric layer on the lower interlayer dielectric. The ferroelectric layer and the bottom electrode are successively patterned to form a plurality of bottom electrodes that are 2-dimensionally arranged along rows and columns and to form a plurality of ferroelectric patterns formed on the bottom electrodes. An insulating pattern is formed to fill gap areas between the ferroelectric layer patterns and between the bottom electrodes. A top

electrode layer is formed on the insulating pattern and the ferroelectric layer patterns. The top electrode layer is patterned to form a common top electrode covering the ferroelectric layer patterns that are arranged on the at least two adjacent rows. The common top electrode is contact with the plate line.

Another method of fabricating the plurality of the ferroelectric capacitors includes a step of forming a plurality of bottom electrodes that are 2-dimensionally arranged on the lower interlayer dielectric along rows and columns. A ferroelectric layer and a top electrode layer are sequentially formed on an entire surface of the semiconductor substrate having the bottom electrodes. The top electrode layer and the ferroelectric layer are patterned to form a common ferroelectric layer pattern and a common top electrode that are sequentially stacked. The common ferroelectric layer pattern covers the bottom electrodes that are arranged on the at least two adjacent rows. Therefore, the common top electrode is interposed between the plate line and the common ferroelectric layer pattern. Preferably, a lower insulating pattern is formed to fill the gap area between the bottom electrodes prior to formation of the ferroelectric layer.

On the other hand, a method of forming the upper interlayer dielectric and the plurality of the plate lines includes a step of forming a bottom plate layer on an entire surface of the semiconductor substrate having the plurality of ferroelectric capacitors. The bottom plate layer is patterned to form a local plate line covering the ferroelectric capacitors that are arranged on at least two adjacent rows. An upper interlayer dielectric is formed on an entire surface of the semiconductor substrate having the local plate line. In this case, the upper interlayer dielectric can be formed by sequentially stacking

first and second upper interlayer dielectrics. Furthermore, a plurality of main wordlines can be formed on the first upper interlayer dielectric in parallel with the column direction prior to formation of the second upper interlayer dielectric. The second upper interlayer dielectric and the first upper interlayer dielectric are successively patterned to additionally form a slit-type via hole that is parallel with the main wordlines. The slit-type via hole penetrates the upper interlayer dielectric between the main wordlines to expose the local plate line. A main plate line is formed to cover the slit-type via hole.

Alternatively, a method of forming the upper interlayer dielectric and the plurality of plate lines includes a step of forming an upper interlayer dielectric on an entire surface of the semiconductor substrate having the plurality of ferroelectric capacitors. The upper interlayer insulating can be formed by sequentially stacking first and second upper interlayer dielectrics. In this case, main wordlines can be formed between the first and second upper interlayer dielectrics in parallel with the column direction. The upper interlayer dielectric is patterned to form a slit-type via hole between the main wordlines in parallel with the column direction. The slit-type via hole exposes upper surfaces of the ferroelectric capacitors that are arranged on at least two adjacent rows. A main plate line is formed to cover the slit-type via hole.

If each of the ferroelectric capacitors comprises the bottom electrode, the ferroelectric pattern, and the top electrode that are sequentially stacked, the slit-type via hole exposes the top electrodes that are arranged on at least two adjacent rows. Preferably, an insulating pattern filling the gap area

between the ferroelectric capacitors is formed of a material layer having an etch selectivity with respect to the upper interlayer dielectric.

Also, if each of the ferroelectric capacitors includes the common top electrode, the slit-type via hole exposes the common top electrode.

Furthermore, each of the bottom electrodes is electrically connected to a predetermined area of the semiconductor substrate through a storage node contact hole penetrating the lower interlayer dielectric. Preferably, an upper diameter of the storage node contact is larger than a lower diameter thereof. And preferably, a hydrogen barrier layer pattern is formed on at least a sidewall of the ferroelectric layer pattern or at least a sidewall of the common ferroelectric layer pattern.

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Like numbers refer to like elements throughout.

A cell array area of a ferroelectric memory device according to the invention is partially illustrated in Fig. 4. And, ferroelectric memory devices according to first to third embodiments of the invention are described with

reference to Fig. 5 through Fig. 7.

Referring now to Fig. 4 and Fig. 5, a device isolation layer 53 is located at a predetermined area of a semiconductor substrate 51 to define a plurality of active regions 53a that are 2-dimensionally arranged. A plurality of insulated gate electrodes 57 (i.e., a plurality of wordlines) are arranged across the active regions 53a and the device isolation layer 53. The gate electrodes 57 are parallel with a row direction (y-axis). Each of the active regions 53a intersects a couple of gate electrodes 57 to divide each of the active regions 53a into three parts. A common drain region 61d is formed at an active region 53a between the pair of the gate electrodes 57. Source regions 61s are formed at active regions 53a that are located at opposite sides of the common drain region 61d. Therefore, cell transistors are formed at points where the gate electrodes 57 intersect the active regions 53a. As a result, the cell transistors are 2-dimensionally arranged along a column direction (x-axis) and a row direction (y-axis).

An entire surface of the semiconductor substrate having the cell transistors is covered with a lower interlayer dielectric 74. Crossing over the wordlines 57, a plurality of bitlines 71 are arranged in the lower interlayer dielectric 74. Each of the bitlines 71 is electrically connected to the common drain region 61d through a bitline contact hole 71a. The source regions 61s are exposed by storage node contact holes 75a that penetrate the lower interlayer dielectric 74. Preferably, an upper sidewall of the storage node contact hole 75a has a sloped profile. Each of the storage node contact holes 75a is filled with contact plugs 75. An upper diameter of the contact plug 75 is larger than a lower diameter thereof, as shown in Fig. 5.

On an entire surface of the semiconductor substrate having the contact plugs, a plurality of ferroelectric capacitors 82 (CP shown in Fig. 4) are 2-dimensionally arranged along the column direction (x-axis) and the row direction (y-axis). Each of the ferroelectric capacitors 32 comprises a bottom electrode 77, a ferroelectric layer pattern 79, and a top electrode 81 that are sequentially stacked. The bottom electrodes 77 are located on the contact plugs 75, respectively. As a result, the bottom electrode 77 is electrically connected to the source region 61s through the contact plug 75. Preferably, a gap area between the ferroelectric capacitors 82 is filled with insulating patterns 85a.

And preferably, a hydrogen barrier layer pattern 83a is interposed between the insulating pattern 85a and the ferroelectric capacitors 82. Preferably, the hydrogen barrier layer pattern 83a is made of titanium oxide (TiO_2), aluminum oxide (Al_2O_3), silicon nitride (Si_3N_4), or combination thereof. This makes it possible to prevent hydrogen atoms from penetrating into the ferroelectric layer pattern 79. If hydrogen atoms are implanted into the ferroelectric pattern 79, a reliability of the ferroelectric pattern 79 is degraded. For example, if hydrogen atoms are injected into a ferroelectric layer such as PZT (Pb, Zr, TiO_3) layer, oxygen atoms in the PZT layer react with the hydrogen atoms to cause an oxygen vacancy therein. Owing to the oxygen vacancy, a polarization characteristic of the ferroelectric layer is deteriorated to cause a malfunction of a ferroelectric memory device.

Furthermore, if the hydrogen atoms are captured in interface traps between the ferroelectric layer pattern and top/bottom electrodes, an energy barrier therebetween is lowered. Accordingly, a leakage current

characteristic of the ferroelectric capacitor is deteriorated. As a result, the hydrogen barrier layer pattern 83a improves characteristic and reliability of the ferroelectric capacitor 82.

A plurality of local plate lines 87 (PL shown in Fig. 4) are arranged on the ferroelectric capacitors 82 and the insulating pattern 85a. Also, the local plate lines 87 are parallel with the row direction (y-axis). Each of the local plate lines 87 covers the ferroelectric capacitors 82 that are arranged on at least two adjacent rows. Thus, the local plate line 87 is directly contact with the top electrodes 81 that are arranged on the at least two adjacent rows. An entire surface of the semiconductor substrate having the local plate lines 87 is covered with an upper interlayer dielectric. In this case, the upper interlayer dielectric may includes first and second upper interlayer dielectrics 89 and 93 that are sequentially stacked.

Furthermore, a plurality of main wordlines 91 may be interposed between the first and second upper interlayer dielectrics 89 and 93. Generally, each of the main wordlines 91 controls four wordlines 57 using a decoder. A main plate line 97 may be arranged in the upper interlayer dielectric between the main wordlines 91. The main plate line 97 is electrically connected to the local plate line 87 through a slit-type via hole 95 penetrating the upper interlayer dielectric. The slit-type via hole 95 is parallel with the row direction (y-axis). A width of the slit-type via hole 95 is larger than a diameter of the via hole (39 of Fig. 3) of the prior art. The local plate line 87 is directly contact with upper surfaces of the top electrodes 81.

A plate line is composed of the local plate line 87 and the main plate

line 97. Also, the plate line may be composed of only the local plate line 87 or only the main plate line 97. Particularly, if the plate line is composed of only the main plate line 97, the insulating pattern 85a is preferably made of material having an etch selectivity with respect to the upper interlayer dielectric. For example, if the upper interlayer dielectric is made of silicon oxide, the insulating pattern 85a is preferably made of silicon nitride.

A ferroelectric memory device according to a second embodiment of the invention is shown in Fig. 6. In the second embodiment, cell transistors, a lower interlayer dielectric, and contact plugs have the same configuration as those in the first embodiment, so that description thereof will be skipped herein.

Referring to Fig. 4 and Fig. 6, a plurality of ferroelectric capacitors covering the contact plugs 75 are located on the lower interlayer dielectric 74. Therefore, the ferroelectric capacitors are 2-dimensionally arranged along the row and column directions. Each of the ferroelectric capacitors comprises a bottom electrode 101, a ferroelectric layer pattern 103, a common top electrode 109 that are sequentially stacked. The common top electrode 109 is extended to cover ferroelectric layer patterns 103 that are arranged on at least two adjacent rows. Therefore, the common top electrode 109 is arranged in parallel with the row direction, similar to a local plate line PL shown in Fig. 4. Preferably, gap areas between the ferroelectric patterns 103 and between the bottom electrodes 101 are filled with a lower insulating pattern 107a. And preferably, a hydrogen barrier layer pattern 105a is interposed between the lower insulating pattern 107a and at least the ferroelectric layer pattern 103, as in the first embodiment.

An entire surface of the semiconductor substrate having the common top electrode 109 is covered with an upper insulating layer 111. The insulating layer 111 has a slit-type contact hole that exposes the common top electrode 109. The slit-type contact hole runs parallel with the row direction (y-axis) and is covered with a local plate line 113 (PL shown in Fig. 4). As a result, the local plate line 113 is electrically connected to the common top electrode 109 through the slit-type contact hole. An entire surface of the semiconductor substrate having the local plate line 113 is covered with an upper interlayer dielectric. The upper interlayer dielectric comprises first and second upper interlayer dielectrics 115 and 119 that are sequentially stacked.

Furthermore, a plurality of main wordlines 117 may be interposed between the first and second upper interlayer dielectrics 115 and 119. The main wordlines 117 are parallel with the row direction. In addition, a main plate line 123 may be located in the upper interlayer dielectric between the main wordlines 117. The main plate line 123 is electrically connected to the local plate line 113 through a slit-type via hole 121 that penetrates the upper interlayer dielectric. The slit-type via hole 121 is parallel with the row direction (y-axis).

A plate line comprises the local plate line 113 and the main plate line 123. Alternatively, the plate line may consist of only the local plate line 113 or only the main plate line 123.

A ferroelectric memory device according to a third embodiment of the invention is shown in Fig. 7. In the third embodiment, cell transistors, a lower interlayer dielectric, and contact plugs have the same configuration as

those in the first embodiment, so that description thereof will be skipped herein.

Referring to Fig. 4 and Fig. 7, a plurality of ferroelectric capacitors covering the contact pugs 75 are arranged on the lower interlayer dielectric 74. Therefore, the ferroelectric capacitors are 2-dimensionally arranged along the row and column directions. Each of the ferroelectric capacitors comprises a bottom electrode 151, a common ferroelectric layer pattern 155, and a common top electrode 157 that are sequentially stacked. The common ferroelectric pattern 155 is extended to cover the bottom electrodes 151 that are arranged on at least two adjacent rows. Also, the common top electrode 157 is stacked on the common ferroelectric layer pattern 155. Therefore, the common ferroelectric pattern 155 and the common top electrode 157 are arranged in parallel with the row direction, similar to a local pate line PL shown in Fig. 4.

Preferably, a gap area between the bottom electrodes 151 is filled with a lower insulating pattern 153a. And preferably, gap areas between the common ferroelectric layer patterns 155 and between the common top electrodes 157 are filled with a top insulating pattern 161. And preferably, a hydrogen barrier layer pattern 159 is interposed between the top insulating pattern 161 and at least the common ferroelectric layer pattern 155.

A local plate line 163 (PL shown in Fig. 4) is located on the common top electrode 157. Also, the local plate line 163 is parallel with the row direction. An entire surface of a semiconductor substrate having the local plate line 163 is covered with an upper interlayer dielectric, which includes first and second upper interlayer dielectrics 165 and 169 that are sequentially

stacked.

Furthermore, a plurality of main wordlines 167 may be interposed between the first and second upper interlayer dielectrics 165 and 169. The main wordlines 167 are parallel with the row direction. In addition, a main plate line 173 may be disposed in the upper interlayer dielectric between the main wordlines 167. The main plate line 173 is electrically connected to the local plate line 163 through a slit-type via hole 171 that penetrates the upper interlayer dielectric. The slit-type via hole 171 is parallel with the row direction (y-axis).

A plate line comprises the local plate line 163 and the mina plate line 173. Unlike this, the plate line may consist of only the local plate line 163 or only the man plate line 173.

A method of fabricating a ferroelectric memory device according to the present invention will now be described more fully hereinafter with reference to Fig. 8 through Fig. 14.

Referring now to Fig. 8, a device isolation layer 53 is formed in a predetermined area of a semiconductor substrate 51 to define a plurality of active regions (53a shown in Fig. 4). A gate insulating layer, a gate conductive layer, and a capping insulating layer are sequentially formed on an entire surface of the semiconductor substrate 51 having the active regions. The capping insulating layer, the gate conductive layer, and the gate insulating layer are successively patterned to form a plurality of gate patterns 60 crossing over the active regions and the device isolation layer 53. Each of the gate patterns 57 comprises a gate insulating pattern 55, a gate electrode 57, and a capping insulating pattern 59 that are sequentially

stacked. Each of the active regions intersects the couple of the gate electrodes 57, which corresponds to a wordline.

Using the gate patterns 60 and the device isolation layer 53 as ion implantation masks, impurities are implanted into the active regions to form three impurity regions in each of the active regions. A central region out of the impurity regions corresponds to a common drain region 61d, and the other regions correspond to source regions 61s. Therefore, a couple of cell transistors are formed in each of the active regions. As a result, the cell transistors are 2-dimensionally arranged on the semiconductor substrate 51 along row and column directions. Then, a spacer 63 is formed on a sidewall of the gate pattern 60 using a conventional manner.

Referring now to Fig. 9, a first lower interlayer dielectric 65 is formed on an entire surface of a semiconductor substrate having the spacer 63. The first lower interlayer dielectric 65 is patterned to form pad contact holes exposing the source/drain regions 61s and 61d. A conventional manner is used to form storage node pads 67s and bitline pads 67d in the pad contact holes. The storage node pads 67s are connected to the source regions 61s, and the bitline pad 67d is connected to the common drain region 61d. A second lower interlayer dielectric 69 is formed on an entire surface of a semiconductor substrate having the pads 67s and 67d. The second lower interlayer dielectric 69 is patterned to form bitline contact holes (71a shown in Fig. 4) exposing the bitline pads 67d. A plurality of parallel bitlines 71 are formed to cover the bitline contact holes, and cross over the wordlines 57.

Referring now to Fig. 10, a third lower interlayer dielectric 73 is formed on an entire surface of a semiconductor substrate having the bitlines

71. The first to third lower interlayer dielectrics 65, 69, and 73 constitute a lower interlayer dielectric 74. The second and third lower interlayer dielectrics 69 and 73 are patterned to form storage node contact holes (75a shown in Fig. 4) exposing the storage node pads 67s. The storage node contact hole may be formed by wet and dry etch process in order to increase an upper diameter thereof. Accordingly, an upper sidewall of the storage node contact hole may have a sloped profile, as shown in the drawing. This is aimed at decreasing in an electrical resistance between a bottom electrode, formed in a subsequent process, and the source region 61s. Contact plugs 75 are formed in the storage node contact holes.

Referring now to Fig. 11, a bottom electrode layer, a ferroelectric layer, and a top electrode layer are sequentially formed on the contact plugs 75 and the lower interlayer dielectric 74. The top electrode layer, the ferroelectric layer, and the bottom electrode layer are successively patterned to form a plurality of ferroelectric capacitors 82 (CP shown in Fig. 4) that are 2-dimensionally arranged along row and column directions. Each of the ferroelectric capacitors 82 includes a bottom electrode 77, a ferroelectric layer pattern 79, and a top electrode 81 that are sequentially stacked. The bottom electrodes 77 are contact with the contact plugs 75, respectively. Thus, the ferroelectric capacitors 82 are electrically connected to the source regions 61s, respectively. An insulating layer 85 is then formed on an entire surface of a resultant structure in which the ferroelectric capacitors 82 are formed. Prior to formation of the insulating layer 85, a hydrogen barrier layer 83 may be formed conformally. Preferably, the hydrogen barrier layer 83 is made of titanium oxide (TiO_2), aluminum oxide (Al_2O_3), silicon nitride

(Si_3N_4), or combination thereof.

Referring now to Fig. 12, the insulating layer 85 and the hydrogen barrier layer 83 are planarized to expose the top electrodes 81. Thus, a hydrogen barrier layer pattern 83a and an insulating pattern 85a are formed between the ferroelectric capacitors 82. The hydrogen barrier layer pattern 83a covers sidewalls of the ferroelectric capacitors 82 (i.e., sidewalls of the ferroelectric layer patterns 79), thereby preventing hydrogen atoms from being injected into the ferroelectric layer patterns 79. If the hydrogen atoms are implanted thereinto, characteristics of ferroelectric capacitors 82 such as a polarization characteristic or a leakage current characteristic are deteriorated. As a result, the hydrogen barrier layer pattern 83a improves characteristics of the ferroelectric capacitors 82.

A bottom plate layer is formed on an entire surface of the semiconductor substrate including the insulating pattern 85a. The bottom plate layer is patterned to form a plurality of local plate lines 87 (PL shown in Fig. 4) that are parallel with the wordlines 57. That is, the local plate lines 87 are parallel with a row direction (y-axis shown in Fig. 4). Each of the local plate lines 87 is directly contact with a plurality of top electrodes 81 that are arranged along two adjacent rows. An upper interlayer dielectric is formed on an entire surface of the semiconductor substrate having the local plate lines 87. The upper interlayer dielectric is formed by sequentially stacking first and second upper interlayer dielectrics 89 and 93. Prior to formation of the second upper interlayer dielectric 93, a plurality of parallel main wordlines 91 may be formed on the first upper interlayer dielectric 89. Conventionally, one main wordline 91 controls four wordlines 57 through a

decoder.

Referring now to Fig. 13, the upper interlayer dielectric is patterned to form a slit-type via hole 95 exposing the local plate line 87. The slit-type via hole 95 is formed between the main wordlines 91 in parallel with the main wordlines 91. Compared with a prior art, the slit-type via hole 95 has greater width, as shown in the drawing. Nevertheless, a spacing (A) between the slit-type via hole 95 and the adjacent main wordlines 91 can be greater, compared with the prior art. This leads to conspicuous decrease in a probability that the slit-type via hole 95 will be exposed, even though the slit-type via hole 95 is formed by wet and dry etch in order to lower an aspect ratio thereof. As a result, the aspect ratio of the slit-type via hole 95 can be lowered conspicuously without exposure of the main wordlines 91, and an exposed area of the local plate line 87 can be maximized.

An top plate layer such as a metal layer is formed on an entire surface of a resultant structure where the slit-type via hole 95 is formed. In this case, the top plate layer has a high step coverage because an aspect ratio of the slit-type via hole 95 is conspicuously low. The top plate layer is patterned to form a main plate line 97 covering the slit-type via hole 95.

A modification of the first embodiment described in Fig. 8 through Fig. 13 will now be described with reference to Fig. 14. This modified embodiment is identical to the first embodiment except a step of forming the local plate line 87. In the modified embodiment, not only the top electrodes 81 but also the insulating pattern 85a therebetween are exposed during formation of the slit-type via hole 95. Accordingly, the insulating pattern 85a is preferably made of material (e.g., silicon nitride) having an etch

selectivity with respect to the upper interlayer dielectric.

The local plate line 87 and the main plate line 97 constitute a plate line. Also, only a local plate line or only a main plate line may constitutes the plate line.

A method of fabricating a ferroelectric memory device according to a second embodiment of the invention will now be described with reference to Fig. 15 through Fig. 19. In the second embodiment, cell transistors, a lower interlayer dielectric, and contact plugs can be formed using the same manner as the first embodiment, so that description thereof will be skipped herein.

Referring now to Fig. 15, a bottom electrode layer and a ferroelectric layer are sequentially formed on the lower interlayer dielectric 74 and the contact plugs 75. The ferroelectric layer and the bottom electrode layer are successively patterned to form a plurality of bottom electrodes 101 covering the contact plugs 75 and a plurality of ferroelectric layer patterns 103 stacked on the bottom electrodes 101. Using the same manner as in the first embodiment, a hydrogen barrier layer 105 and a lower insulating layer 107 are sequentially formed on an entire surface of a semiconductor substrate having the ferroelectric layer patterns 103.

Referring now to Fig. 16, the lower insulating layer 107 and the hydrogen barrier layer 105 are planarized to expose the ferroelectric layer patterns 103. Thus, a lower insulating pattern 107a and a hydrogen barrier layer pattern 105a are formed in gap areas between the ferroelectric layer patterns 103 and between the bottom electrodes 101. A top electrode layer is formed on an entire surface of a resultant structure in which the lower insulating pattern 107a and the hydrogen barrier layer pattern 105a are

formed. The top electrode layer is patterned to form a plurality of common top electrodes 109 that are parallel with the wordlines 57. Each of the common top electrodes 109 covers the ferroelectric layer patterns 103 that are arranged on at least two adjacent rows.

Referring now to Fig. 17, an upper insulating layer 111 is formed on an entire surface of a semiconductor substrate including the common top electrodes 109. The upper insulating layer 111 is patterned to form a slit-type contact hole exposing the common top electrode 109. A bottom plate layer is formed on an entire surface of a semiconductor substrate having the slit-type contact hole. The bottom plate layer is patterned to form a local plate line 113 (PL shown in Fig. 4) covering the slit-type contact hole. First and second upper interlayer dielectrics 113 and 119 are sequentially formed on an entire surface of the semiconductor substrate including the local plate line. The first and second upper interlayer dielectrics 113 and 119 compose an upper interlayer dielectric.

Furthermore, a plurality of main wordlines 117 may be formed between the first and second interlayer dielectrics 113 and 119. The main wordlines 117 are formed by the same manner as in the first embodiment of the present invention.

Referring now to Fig. 18, a slit-type via hole 121 is formed which penetrates the upper interlayer dielectric. Then, a main plate line 123 is formed which covers the slit-type via hole 121. The slit-type via hole 121 and the main plate line 123 are formed by the same manner as in the first embodiment of the present invention.

A modification of the second embodiment described in Fig. 15

through Fig. 18 will now be described with reference to Fig. 19. The modified second embodiment is identical to the second embodiment except a step of forming the local plate line 115. In this case, the slit-type via hole 121 exposes the common top electrode 109.

A method of fabricating a ferroelectric memory device according to a third embodiment of the invention will now be described with reference to Fig. 20 through Fig. 24. In the third embodiment, cell transistors, a lower interlayer dielectric, and contact plugs are formed by the same manner as in the first embodiment, so that description thereof will be skipped herein.

Referring now to Fig. 20, a bottom electrode layer is formed on the lower interlayer dielectric 74 and the contact plugs 75. The bottom electrode layer is patterned to for a plurality of bottom electrodes 151 covering the contact plugs 75. A lower insulating layer 153 is formed on an entire surface of a semiconductor substrate including the bottom electrodes 151.

Referring now to Fig. 21, the lower insulating layer 153 is planarized to expose upper surfaces of the bottom electrodes 151. Thus, the lower insulating pattern 153a is formed in a gap area between the bottom electrodes 151. A ferroelectric layer and a top electrode layer are sequentially formed on an entire surface of a resulting structure in which the lower insulating pattern 153a is formed. The top electrode layer and the ferroelectric layer are successively patterned to form a plurality of common ferroelectric layer patterns 155 that are parallel with the wordlines 57 and a plurality of common top electrodes 157 that are stacked on the common ferroelectric layer patterns 155. Each of the common ferroelectric layer patterns 155 covers the bottom electrodes 151 that are arranged on at least

two adjacent rows. Using the same manner as in the first embodiment, a hydrogen barrier layer pattern 159 and an upper insulating pattern 161 are formed in gap areas between the common ferroelectric patterns 155 and between the common top electrodes 157.

Referring now to Fig. 22, a bottom plate layer is formed on an entire surface of a semiconductor substrate having the upper insulating pattern 161. The bottom plate layer is patterned to form a local plate line 163 (PL shown in Fig. 4) covering the common top electrode 163. An upper interlayer dielectric is formed on an entire surface of a resultant structure in which the local plate line 163 is formed. The upper interlayer dielectric is formed by sequentially stacking first and second upper interlayer dielectrics 165 and 169. Furthermore, a plurality of parallel main wordlines 167 may be formed between the first and second upper interlayer dielectrics 165 and 169. The main wordlines 167 is formed by the same manner as in the first embodiment described in Fig. 12.

Referring now to Fig. 23, a slit-type via hole 171 is formed which penetrates the upper interlayer dielectric, and a main plate line 173 is formed which covers the slit-type via hole 171. The slit-type via hole 171 and the main plate line 173 are formed by the same manner as in the first embodiment of the invention.

A modification of the third embodiment will now be described with reference to Fig. 24. The modified embodiment is identical to the third embodiment except a step of forming the local plate line 163. In this case, the slit-type via hole 171 exposes the common top electrode 157.

Fig. 25 is a top plan view for explaining a modified version of the

first embodiment described in Fig. 4. Fig. 26 illustrates cross-sectional views, taken along a line II-II' of Fig. 25, for explaining a ferroelectric memory device according to the modified embodiment and a method for fabricating the same. In this modified embodiment, cell transistors, a lower interlayer dielectric, contact plugs, ferroelectric capacitors, and insulating patterns are formed by means of the same method as in the first embodiment described in Fig. 8 through Fig. 11 and will not be described in further detail.

A ferroelectric memory device according to the modified embodiment will now be described with reference to Fig. 25 and Fig. 26.

Referring to Fig. 25 and Fig. 26, a plurality of local plate patterns PP are disposed on the ferroelectric capacitors 82 and the insulating pattern 85a. The local plate patterns PP may be made of one selected from the group consisting of metal, conductive metal oxide, conductive metal nitride and combinations thereof. Specifically, the local plate patterns PP may be made of one selected from the group consisting of, for example, titanium aluminum nitride (TiAlN), titanium (Ti), titanium nitride (TiN), iridium (Ir), iridium oxide (IrO_2), platinum (Pt), ruthenium (Ru), ruthenium oxide (RuO_2), aluminum (Al), and combinations thereof. The local plate patterns PP are 2-dimensionally arranged in the row direction (y-axis) and the column direction (x-axis). More specifically, each of the local plate patterns PP covers the ferroelectric capacitors 82 disposed in at least two adjacent rows and at least one column. For example, each of the local plate patterns PP covers four capacitors 82 disposed in two adjacent rows and two adjacent columns, as illustrated in Fig. 25. As a result, each of the local plate patterns PP becomes in direct contact with the top electrodes 81 disposed in at least

two adjacent rows and at least one column. An entire surface of a semiconductor substrate including the local plate patterns PP is covered with an upper interlayer dielectric. Here, the upper interlayer dielectric may include a first interlayer dielectric 89 and a second interlayer dielectric 93 that are stacked in the order named.

In addition, as described in the first embodiment, a plurality of main wordlines 91 may be interposed between the first and second interlayer dielectrics 89 and 93. Generally, each of the main wordlines 91 controls four wordlines through a decoder. A main plate line 97 is disposed in the upper interlayer dielectric between the main wordlines 91. The main plate line 97 is electrically connected to the local plate patterns PP, disposed in parallel with the y-direction, through a plurality of via holes penetrating the upper interlayer dielectric. Alternatively, the main plate line 97 may be electrically connected to the local plate patterns PP, disposed in parallel with the y-direction, through a slit-type via hole (95 of Fig. 4) penetrating the upper interlayer dielectric.

A method for fabricating a ferroelectric memory device according to the modified embodiment will now be described below.

Referring to Fig. 25 and Fig. 26 again, a bottom plate layer is formed on an entire surface of a semiconductor substrate where the ferroelectric capacitors 82 and insulating patterns 85a are formed. The bottom plate layer may be made of one selected from the group consisting of titanium aluminum nitride (TiAlN), titanium (Ti), titanium nitride (TiN), iridium (Ir), iridium oxide (IrO_2), platinum (Pt), ruthenium (Ru), ruthenium oxide (RuO_2), aluminum (Al), and combinations thereof. The bottom plate layer is

patterned to form a plurality of local plate patterns PP. Each of the local plate patterns PP covers ferroelectric capacitors 82 arranged in at least two adjacent rows and two adjacent columns. For example, each of the local plate patterns PP may more dramatically reduce a physical stress caused by the local plate patterns PP than in the first embodiment adopting local plate lines. Particularly, in the event that the bottom plate layer is made of a high stress material such as iridium and/or iridium oxide, the stress caused by the local plate pattern PP is much lower than the stress caused by the local late lines 87 in the first embodiment. Thus, in the event that the local plate patterns PP is formed instead of the local plate lines 87, a stress applied to the ferromagnetic capacitors 82 may be reduced. As a result, it is possible to suppress degradation in ferroelectric characteristics of the ferroelectric capacitors 82.

An upper interlayer dielectric is formed on an entire surface of a semiconductor substrate including the local plate patterns PP. The formation of the upper interlayer dielectric is done by sequentially stacking first and second upper interlayer dielectrics 89 and 93. Prior to formation of the second upper interlayer dielectric 93, a plurality of main wordlines 91 may be formed on the first upper interlayer dielectric 89 to be parallel with the y-axis. Generally, each of the main wordlines 91 controls four wordlines 57 through a decoder.

Continuously, the upper interlayer dielectric is patterned to form a plurality of via holes 95c exposing the local plate patterns PP. Thus, the via holes 95c are 2-dimensionally arranged in the x-axis and the y-axis. Alternatively, a slit-type via hole (95 of Fig. 5 and Fig. 13) described in the

first embodiment may be formed instead of the via holes 95c. A top plate layer is formed on an entire surface of a semiconductor substrate including the via holes 95c. The top plate layer may be a metal layer and is patterned to form a main plate line 97 covering the via holes 95c. The main plate line 97 is formed to be parallel with the y-axis.

The present invention is not limited to the above-described embodiments and may be modified and changed by those skilled in the art. For example, each of the plate lines may cover ferroelectric capacitors arranged on at least three adjacent rows.

[Effect of the Invention]

As explained so far, one plate line is directly contact with top electrodes of ferroelectric capacitors that are arranged on at least two adjacent rows in a cell array area. Alternatively, ferroelectric capacitors arranged on at least two adjacent rows can share one top common electrode. In this case, the common top electrode is contact with one plate line. Thus, a reliable contact structure can be realized between the plate line and the top electrode.

Further, in the event that main wordlines are arranged in the cell array area and a slit-type via hole is formed between the main wordlines, a spacing between the slit-type via hole and the main wordline can conspicuously increase, compared with a prior art.

Moreover, in the event that a plurality of local plate patterns are formed instead of the local plate line, a physical stress applied to the ferroelectric capacitors can be reduced dramatically. Therefore, it is possible

to suppress degradation in ferroelectric characteristics of ferroelectric capacitors.

As a result, it is possible to increase integration level of ferroelectric memory devices and improve reliability thereof.

WHAT IS CLAIMED IS:

[Claim 1]

A ferroelectric memory device comprising:

a lower interlayer dielectric formed on a semiconductor substrate;

a plurality of ferroelectric capacitors 2-dimensionally arranged on the lower interlayer dielectric along row and column directions;

an upper interlayer dielectric stacked on an entire surface of the semiconductor substrate having the plurality of ferroelectric capacitors; and

a plurality of plate lines arranged in the upper interlayer dielectric in parallel with the row direction,

wherein each of the plate lines is directly contact with upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows.

[Claim 2]

The ferroelectric memory device of claim 1, wherein the plate line is a local plate line directly contact with the upper surfaces of the ferroelectric capacitors arranged on the at least two adjacent rows, the local plate line being covered with the upper interlayer dielectric.

[Claim 3]

The ferroelectric memory device of claim 1, wherein the plate line is a main plate line directly contact with the ferroelectric capacitors arranged on the at least two adjacent rows through a slit-type via hole penetrating the upper interlayer dielectric.

[Claim 4]

The ferroelectric memory device of claim 3, wherein the upper interlayer dielectric includes first and second upper interlayer dielectrics which are sequentially stacked.

[Claim 5]

The ferroelectric memory device of claim 4, further comprising main wordlines interposed between the first and second upper interlayer dielectrics, wherein the main wordlines are arranged at opposite sides of the slit-type via hole in parallel with the row direction.

[Claim 6]

The ferroelectric memory device of claim 1, wherein the plate line includes:

a local plate line being in directly connect with upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows, the local plate line being covered with the upper interlayer dielectric; and

a main plate line directly contact with an upper surface of the local plate line through s slit-type via hole penetrating the upper interlayer dielectric.

[Claim 7]

The ferroelectric memory device of claim 6, wherein the upper interlayer dielectric includes first and second upper interlayer dielectric which are sequentially stacked.

[Claim 8]

The ferroelectric memory device of claim 7, further comprising main wordlines interposed between the first and second upper interlayer dielectrics, wherein the main wordlines are arranged at opposite sides of the slit-type via hole in parallel with the row direction.

[Claim 9]

The ferroelectric memory device of claim 1, wherein each of the ferroelectric capacitors is electrically connected to a predetermined area of the semiconductor substrate through a storage node contact hole penetrating the lower interlayer dielectric, an upper diameter of the storage node contact hole being greater than a lower diameter thereof.

[Claim 10]

The ferroelectric memory device of claim 1, wherein each of the ferroelectric capacitors includes a bottom electrode, a ferroelectric layer pattern, and a top electrode which are sequentially stacked, the plate line being directly contact with the top electrodes arranged on at least two adjacent rows.

[Claim 11]

The ferroelectric memory device of claim 10, further comprising an insulating pattern filling a gap area between the ferroelectric capacitors, wherein the insulating pattern is interposed between the upper and lower interlayer dielectrics.

[Claim 12]

The ferroelectric memory device of claim 11, wherein the insulating pattern has an etch selectivity with respect to the upper interlayer dielectric.

[Claim 13]

The ferroelectric memory device of claim 11, further comprising a hydrogen barrier layer pattern interposed between the ferroelectric capacitors and the insulating pattern.

[Claim 14]

The ferroelectric memory device of claim 1, wherein the ferroelectric capacitor includes a bottom electrode, a ferroelectric layer pattern, and a common top electrode, the common top electrode being extended to cover the ferroelectric layer patterns located under the plate line, and an upper surface of the common top electrode being directly contact with the plate line.

[Claim 15]

The ferroelectric memory device of claim 14, further comprising an insulating pattern filling gap areas between the bottom electrodes and between the ferroelectric layer patterns, wherein the insulating pattern is interposed between the upper and lower interlayer dielectrics.

[Claim 16]

The ferroelectric memory device of claim 15, further comprising a

hydrogen barrier layer pattern interposed between at least sidewalls of the ferroelectric layer patterns and the insulating pattern.

[Claim 17]

The ferroelectric memory device of claim 1, wherein the ferroelectric capacitor includes a bottom electrode, a common ferroelectric layer pattern, and a common top electrode, the common ferroelectric layer pattern being extended to cover the bottom electrodes under the plate line, and the common top electrode being interposed between the common ferroelectric layer pattern and the plate line.

[Claim 18]

The ferroelectric memory device of claim 17, further comprising an insulating pattern filling gap areas between the common ferroelectric layer patterns and between the common top electrodes, wherein the insulating pattern is interposed between the lower and upper interlayer dielectrics.

[Claim 19]

The ferroelectric memory device of claim 18, further comprising a hydrogen barrier layer pattern interposed between at least sidewalls of the common ferroelectric layer patterns and the insulating pattern.

[Claim 20]

A ferroelectric memory device comprising:

a plurality of cell transistors 2-dimensionally arranged on a

semiconductor substrate along row and column directions;

a lower interlayer dielectric covering an entire surface of the semiconductor substrate having the cell transistors;

a plurality of ferroelectric capacitors 2-dimensionally arranged on the lower interlayer dielectric along the row and column directions, the ferroelectric capacitors being electrically connected to the cell transistors through storage node contact holes penetrating the lower interlayer dielectric, respectively;

a plurality of local plate lines arranged on the semiconductor substrate having the ferroelectric capacitors in parallel with the row direction, each of the local plate lines being in directly contact with upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows; and

first and second interlayer dielectrics sequentially stacked on an entire surface of the semiconductor substrate having the plurality of local plate lines.

[Claim 21]

The ferroelectric memory device of claim 20, further comprising:

a slit-type via hole penetrating the first and second upper interlayer dielectrics to expose the local plate line; and

a main plate line covering the slit-type via hole.

[Claim 22]

The ferroelectric memory device of claim 21, further comprising a

plurality of main wordlines interposed between the first and second upper interlayer dielectrics, the main wordlines being arranged at opposite sides of the slit-type via hole in parallel with the row direction.

[Claim 23]

The ferroelectric memory device of claim 20, wherein the ferroelectric capacitor includes a bottom electrode, a ferroelectric layer pattern, and a top electrode which are sequentially stacked, the local plate line being in directly contact with the top electrodes arranged on at least two adjacent rows.

[Claim 24]

The ferroelectric memory device of claim 20, wherein the ferroelectric capacitor includes a bottom electrode, a ferroelectric layer pattern, and a common top electrode, the common top electrode being extended to cover the ferroelectric layer patterns located under the local plate line, and an upper surface of the common top electrode being in directly contact with the local plate line.

[Claim 25]

The ferroelectric memory device of claim 20, wherein the ferroelectric capacitor includes a bottom electrode, a common ferroelectric layer pattern, and a common top electrode which are sequentially stacked, the common ferroelectric layer pattern being extended to cover the bottom electrode under the local plate line, and the common top electrode being

interposed between the common ferroelectric layer pattern and the local plate line.

[Claim 26]

A ferroelectric memory device comprising:

a plurality of cell transistors 2-dimensionally arranged on a semiconductor substrate along row and column directions;

a lower interlayer dielectric covering an entire surface of a semiconductor substrate having the cell transistors;

a plurality of ferroelectric capacitors 2-dimensionally arranged on the lower interlayer dielectric along the row and column directions, the ferroelectric capacitors being electrically connected to the cell transistors through storage node contact holes penetrating the lower interlayer dielectric, respectively;

first and second upper interlayer dielectrics sequentially stacked on an entire surface of the semiconductor substrate having the ferroelectric capacitors;

a slit-type via hole penetrating the first and second upper interlayer dielectrics to expose upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows, the slit-type via hole being parallel with the row direction; and

a main plate line covering the slit-type via hole.

[Claim 27]

The ferroelectric memory device of claim 26, further comprising a

plurality of main wordlines arranged at opposite sides of the slit-type via hole in parallel with the row direction, wherein the main wordlines are interposed between the first and second upper interlayer dielectrics.

[Claim 28]

The ferroelectric memory device of claim 26, wherein the ferroelectric capacitor includes a bottom electrode, a ferroelectric layer pattern, and a top electrode which are sequentially stacked, the main plate line being directly contact with the top electrodes arranged on at least two adjacent rows.

[Claim 29]

The ferroelectric memory device of claim 26, wherein the ferroelectric capacitor includes a bottom electrode, a ferroelectric layer pattern, and a common top electrode which are sequentially stacked, the common top electrode being extended to cover the ferroelectric layer patterns located under the man plate line, and an upper surface of the common top electrode being directly contact with the main plate line.

[Claim 30]

The ferroelectric memory device of claim 26, wherein the ferroelectric capacitor includes a bottom electrode, a common ferroelectric layer pattern, and a common top electrode which are sequentially stacked, the common ferroelectric layer pattern being extended to cover the bottom electrodes under the main plate line, and the common top electrode being

interposed between the common ferroelectric layer pattern and the main plate line.

[Claim 31]

A method of fabricating a ferroelectric memory device, comprising the steps of:

forming a lower interlayer dielectric on a semiconductor substrate;

forming a plurality of ferroelectric capacitors 2-dimensionall arranged on the lower interlayer dielectric along row and column directions; and

forming an upper interlayer dielectric stacked on an entire surface of the semiconductor substrate having the ferroelectric capacitors and a plurality of plate lines formed in the upper interlayer dielectric, each of the plate lines being directly contact with upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows.

[Claim 32]

The method of claim 31, wherein the step of forming the plurality of ferroelectric capacitors comprises:

sequentially forming a bottom electrode layer, a ferroelectric layer, and a top electrode layer on the lower interlayer dielectric; and

patterning the top electrode layer, the ferroelectric layer, and the bottom electrode layer to form a plurality of bottom electrodes 2-dimensionally arranged along the row and column directions, a plurality of ferroelectric layer patterns stacked on the bottom electrodes, and a plurality

of top electrodes stacked on the ferroelectric layer patterns.

[Claim 33]

The method of claim 32, wherein the step of forming the upper interlayer dielectric and the plate lines comprises:

forming an insulating layer on an entire surface of the semiconductor substrate in which the ferroelectric capacitors are formed;

planarizing the insulating layer down to surfaces of the top electrodes to form an insulating pattern filling a gap area between the ferroelectric capacitors;

forming a bottom plate layer on an entire surface of the semiconductor substrate having the insulating pattern;

patterning the bottom plate layer to form a plurality of local plate lines in parallel with the row direction, each of the local plate lines being directly contact with the top electrodes arranged on at least two adjacent rows; and

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate having the local plate lines.

[Claim 34]

The method of claim 33, further comprising a step of conformally forming a hydrogen barrier layer on an entire surface of the substrate having the ferroelectric capacitors prior to the step of forming the insulating layer, wherein the hydrogen barrier layer on the top electrodes is removed while planarizing the insulating layer.

[Claim 35]

The method of claim 33, further comprising the steps of:

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing the local plate line in parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 36]

The method of claim 35, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 37]

The method of claim 32, wherein the step of forming the upper interlayer dielectric and the plate lines comprises the steps of:

forming an insulating layer on an entire surface of the semiconductor substrate in which the ferroelectric capacitors are formed;

planarizing the insulating layer down to surfaces of the top electrodes to form an insulating pattern filling a gap area between the ferroelectric capacitors;

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate having the insulating pattern;

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing the top electrodes arranged on at least two adjacent rows in parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 38]

The method of claim 37, wherein the insulating layer is made of material having an etch selectivity with respect to the first upper interlayer dielectric.

[Claim 39]

The method of claim 37, further comprising a step of conformally forming a hydrogen barrier layer on an entire surface of the semiconductor substrate having the ferroelectric capacitors prior to the step of forming the insulating layer, wherein the hydrogen barrier layer on the top electrodes is removed while planarizing the insulating layer.

[Claim 40]

The method of claim 37, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to the step of forming the second upper interlayer dielectric, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 41]

The method of claim 31, wherein the step of forming the ferroelectric

capacitors comprises the steps of:

sequentially forming a bottom electrode layer and a ferroelectric layer on the lower interlayer dielectric;

successively patterning the ferroelectric layer and the bottom electrode layer to form a plurality of bottom electrodes 2-dimensionally arranged along the row and column directions and a plurality of ferroelectric layer patterns stacked on the bottom electrodes;

forming a lower insulating pattern filling gap areas between the bottom electrodes and between the ferroelectric layer patterns;

forming a top electrode layer on an entire surface of the semiconductor substrate having the lower insulating pattern; and

patterning the top electrode layer to form a plurality of common top electrodes in parallel with the row direction, each of the common top electrodes being directly contact with the ferroelectric layer patterns arranged on at least two adjacent rows.

[Claim 42]

The method of claim 41, further comprising a step of forming a hydrogen barrier layer pattern interposed between a sidewall of the ferroelectric layer pattern and the lower insulting layer pattern.

[Claim 43]

The method of claim 41, wherein the step of forming the upper interlayer dielectric and the plate lines comprises:

forming an upper insulating layer on an entire surface of the

semiconductor substrate in which the ferroelectric capacitors are formed;

patterning the upper insulating layer to form a slit-type contact hole exposing the common top electrode in parallel with the row direction;

forming a local plate line covering the slit-type contact hole; and

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate having the local plate line.

[Claim 44]

The method of claim 43, further comprising the steps of:

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing the local plate line in parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 45]

The method of claim 44, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to the step of forming the second upper interlayer dielectric, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 46]

The method of claim 41, wherein the step of forming the plate lines and the upper interlayer dielectric comprises:

sequentially forming first and second upper interlayer dielectrics on

an entire surface of the semiconductor substrate in which the ferroelectric capacitors are formed;

successively patterning the first and second upper interlayer dielectrics to form a slit-type via hole exposing the common top electrode in parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 47]

The method of claim 46, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to the step of forming the second upper interlayer dielectric, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 48]

The method of claim 31, wherein the step of forming the ferroelectric capacitors comprises:

forming a plurality of bottom electrodes 2-dimensionally arranged on the lower interlayer dielectric along the row and column directions;

sequentially forming a ferroelectric layer and a top electrode layer on an entire surface of the semiconductor substrate having the bottom electrodes;

sequentially patterning the top electrode layer and the ferroelectric layer to form a plurality of common ferroelectric layer patterns in parallel with the row direction and a plurality of common top electrodes stacked on

the plurality of ferroelectric patterns, the common ferroelectric layer patterns being directly contact with upper surfaces of the bottom electrodes arranged on at least two adjacent rows.

[Claim 49]

The method of claim 48, wherein the step of forming the upper interlayer dielectric and the plate lines comprises:

forming an insulating pattern filling a gap area between the ferroelectric capacitors;

forming a bottom plate layer on an entire surface of the semiconductor substrate having the insulating pattern;

patterning the bottom plate layer to form a plurality of local plate lines covering the common top electrodes; and

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate having the local plate lines.

[Claim 50]

The method of claim 49, further comprising a step of forming a hydrogen barrier layer pattern interposed between at least the common ferroelectric layer pattern and the insulating pattern.

[Claim 51]

The method of claim 49, further comprising the steps of:

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing the local plate line in

parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 52]

The method of claim 51, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to formation of the second upper interlayer dielectric, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 53]

The method of claim 48, wherein the step of forming the upper interlayer dielectric and the plate lines comprises:

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate in which the ferroelectric capacitors are formed;

successively patterning the second and first interlayer dielectrics to form a slit-type via hole exposing the common top electrode in parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 54]

The method of claim 53, further comprising a step of forming an insulating pattern filling the gap area between the ferroelectric capacitors prior to formation of the first upper interlayer dielectric.

[Claim 55]

The method of claim 54, further comprising a step of forming a hydrogen barrier layer pattern interposed between the at least the common ferroelectric layer pattern and the insulating pattern.

[Claim 56]

The method of claim 53, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to formation of the second upper interlayer dielectric, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 57]

A method of fabricating a ferroelectric memory device, comprising the steps of:

forming a plurality of cell transistors 2-dimensionally arranged on a semiconductor substrate along row and column directions;

forming a lower interlayer dielectric on an entire surface of the semiconductor substrate having the cell transistors;

forming a plurality of ferroelectric capacitors 2-dimensionally arranged on the lower interlayer dielectric along the row and column directions, the ferroelectric capacitors being electrically connected to the cell transistors through storage node contact holes penetrating the lower interlayer dielectric, respectively;

forming a plurality of local plate lines on the semiconductor substrate having the plurality of the ferroelectric capacitors in parallel with the row direction, each of the local plate lines being directly contact with upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows; and

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate having the plurality of local plate lines.

[Claim 58]

The method of claim 57, wherein the step of forming the plurality of the local plate lines comprises the steps of:

forming an insulating pattern filling a gap area between the plurality of the ferroelectric capacitors;

forming a bottom plate layer on an entire surface of the semiconductor substrate having the insulating pattern;

patterning the bottom plate layer to form a plurality of local plate lines in parallel with the row direction, each of the local plate lines being directly contact with upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows.

[Claim 59]

The method of claim 57, further comprising the steps of:

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing the local plate line in

parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 60]

The method of claim 59, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to formation of the second upper interlayer dielectric, wherein the man wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 61]

A method of fabricating a ferroelectric memory device, comprising the steps of:

forming a plurality of cell transistors 2-dimensionally arranged on a semiconductor substrate along row and column directions;

forming a lower interlayer dielectric on an entire surface of the semiconductor substrate having the cell transistors;

forming a plurality of ferroelectric capacitors 2-dimensionally arranged on the lower interlayer dielectric along the row and column directions, the ferroelectric capacitors being electrically connected to the cell transistors through storage node contact holes penetrating the lower interlayer dielectric;

sequentially forming first and second upper interlayer dielectrics on an entire surface of the semiconductor substrate having the plurality of ferroelectric capacitors;

successively patterning the second and first upper interlayer dielectrics to form a slit-type via hole exposing upper surfaces of the ferroelectric capacitors arranged on at least two adjacent rows in parallel with the row direction; and

forming a main plate line covering the slit-type via hole.

[Claim 62]

The method of claim 61, further comprising a step of forming a plurality of main wordlines on the first upper interlayer dielectric in parallel with the row direction prior to formation of the second upper interlayer dielectric, wherein the main wordlines are arranged at opposite sides of the slit-type via hole.

[Claim 63]

A method for fabricating a ferroelectric memory device, comprising the steps of:

forming a plurality of cell transistors on a semiconductor substrate to be 2-dimensionally arranged in a row direction and a column direction;

forming a lower interlayer dielectric on an entire surface of a semiconductor substrate including the cell transistors;

forming a plurality ferroelectric capacitors on the lower interlayer dielectric to be 2-dimensionally arranged in the row direction and the column direction, wherein each of the ferroelectric capacitors is electrically connected to each of the cell transistors through a storage node contact hole penetrating the lower interlayer dielectric;

forming a plurality of local plate lines on a semiconductor substrate including the ferroelectric capacitors to be parallel with the row direction, wherein each of the local plate lines directly contacts top surfaces of the ferroelectric capacitors arranged on at least adjacent two rows; and

sequentially forming first and second upper interlayer dielectrics on an entire surface of a semiconductor substrate including the local plate lines.

[Claim 64]

The method of claim 63, wherein each of the local plate lines is made of titanium aluminum nitride, titanium, titanium nitride, iridium, iridium oxide, platinum, ruthenium, ruthenium oxide, aluminum, and combinations thereof.

[Claim 65]

The method of claim 63, wherein the step of forming the local plate lines comprises:

forming an insulating pattern to fill a gap region between the ferroelectric capacitors;

forming a bottom plate layer on an entire surface including the ferroelectric capacitors; and

patterning the bottom plate layer to form a plurality of local plate lines in parallel with the row direction, wherein each of the local plate lines directly contacts top surfaces of the ferroelectric capacitors arranged on at least two adjacent rows.

[Claim 66]

The method of claim 63, further comprising steps:

successively patterning the second interlayer dielectric and the first interlayer dielectric to expose the local plate line and form a slit-type via hole disposed in parallel with the row direction; and

forming a main plate line to cover the slit-type via hole.

[Claim 67]

The method of claim 66, further comprising a step before forming the second upper interlayer dielectric:

forming a plurality of wordlines on the first upper interlayer dielectric to be parallel with the row direction, the wordlines being disposed at opposite sides of the slit-type via hole.

[Claim 68]

A method for fabricating a ferroelectric memory device, comprising:

forming a plurality of cell transistors on a semiconductor substrate to be 2-dimensionally arranged in a row direction and a column direction;

forming a lower interlayer dielectric on an entire surface of a semiconductor substrate including the cell transistors;

forming a plurality of ferroelectric capacitors on the lower interlayer dielectric to be 2-dimensionally arranged in the row direction and the column direction, wherein each of the ferroelectric capacitors is electrically connected to each of the cell transistors through a storage node contact penetrating the lower interlayer dielectric;

sequentially forming first and second upper interlayer dielectrics on an entire surface of a semiconductor substrate including the ferroelectric capacitors;

successively patterning the second upper interlayer dielectric and the first upper interlayer dielectric to expose top surfaces of the ferroelectric capacitors arranged on at least two adjacent rows and form a slit-type via hole disposed in parallel with the row direction; and

forming a main plate line to cover the slit-type via hole.

[Claim 69]

The method of claim 68, further comprising a step before the second upper interlayer dielectric:

forming a plurality of main wordlines on the first upper interlayer dielectric to be parallel with the row direction, the main wordlines being disposed at opposite sides of the slit-type via hole.

[Claim 70]

A ferroelectric memory device comprising:

a semiconductor substrate;

a plurality of ferroelectric capacitors arranged 2-dimensionally on the semiconductor substrate in a row direction and a column direction; and

a plurality of local plate patterns arranged 2-dimensionally in the row direction and the column direction to cover the ferroelectric capacitors,

wherein each of the local plate patterns directly contacts top surfaces of ferroelectric capacitors arranged in at least two adjacent rows and at least

two adjacent columns.

[Claim 71]

The ferroelectric memory device of claim 70, wherein each of the local plate patterns is made of one selected from the group consisting of titanium aluminum nitride, titanium, titanium nitride, iridium, iridium oxide, platinum, ruthenium, ruthenium oxide, aluminum, and combinations thereof.

[Claim 72]

The ferroelectric memory device of claim 70, wherein each of the ferroelectric capacitors includes a bottom electrode, a ferroelectric pattern, and a top electrode that are stacked in the order named, and each of the local plate patterns directly contacts top surfaces of top electrodes arranged in the at least two adjacent rows and the at least two adjacent columns.

[Claim 73]

The ferroelectric memory device of claim 72, wherein each of the local plate patterns directly contacts top surfaces of four top electrodes arranged in at least two adjacent rows and at least two adjacent columns.

[Claim 74]

The ferroelectric memory device of claim 70, further comprising a plurality of main plate lines arranged on a semiconductor substrate including the local plate patterns to be parallel with the row direction, wherein each of the main plate lines is electrically connected to the local plate patterns

arranged in the row direction.

[Claim 75]

The ferroelectric memory device of claim 74, wherein each of the main plate lines is electrically connected to the local plate patterns through a plurality of via holes arranged in parallel with the row direction or a slit-type via hole.

[Claim 76]

The ferroelectric memory device of claim 75, further comprising main wordlines arranged in opposite sides of the slit-type via hole or the via holes to be parallel with the row direction, the main wordlines being disposed over the local plate patterns and under the main plate lines.

[Claim 77]

The ferroelectric memory device of claim 1, wherein the plate line contacts the ferroelectric capacitors arranged in at least two adjacent rows and at least one column.

[Claim 78]

The ferroelectric memory device of claim 4, wherein the slit-type via hole exposes the ferroelectric capacitors arranged in at least two adjacent rows and at least one column.

[Claim 79]

The ferroelectric memory device of claim 7, wherein the slit-type via hole exposes the local plate line on the ferroelectric capacitors arranged in at least two adjacent rows and at least one column.

[Claim 80]

The ferroelectric memory device of claim 34, wherein the plate line contacts top surfaces of the ferroelectric capacitors arranged in at least two adjacent rows and at least one column.

[Claim 81]

The ferroelectric memory device of claim 39, wherein the slit-type via hole exposes the local plate line on the ferroelectric capacitors arranged in at least two adjacent rows and at least one column.

FIG. 1

(PRIOR ART)

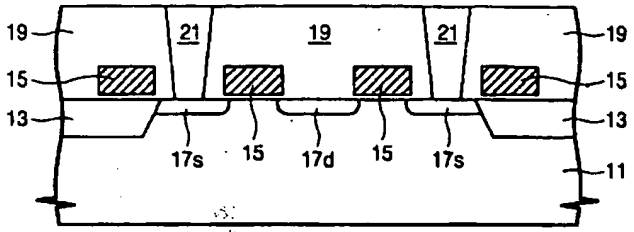

FIG. 2

(PRIOR ART)

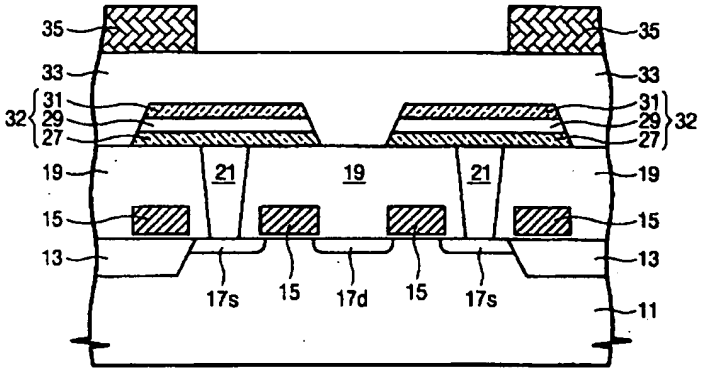

FIG. 3

(PRIOR ART)

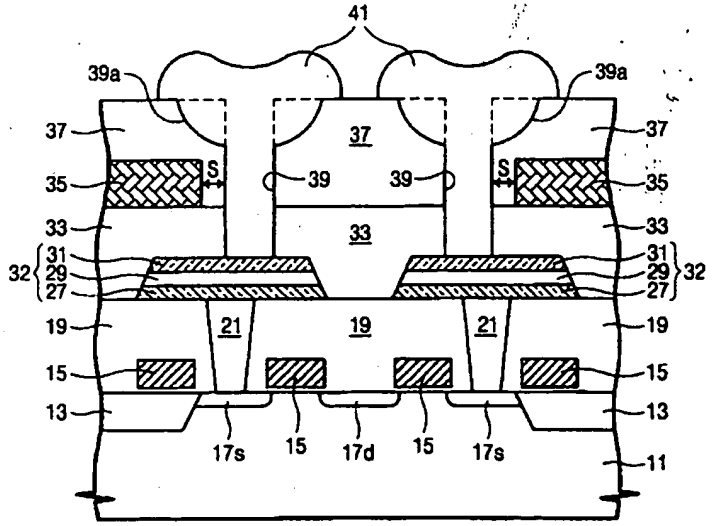

FIG. 1

(PRIOR ART)

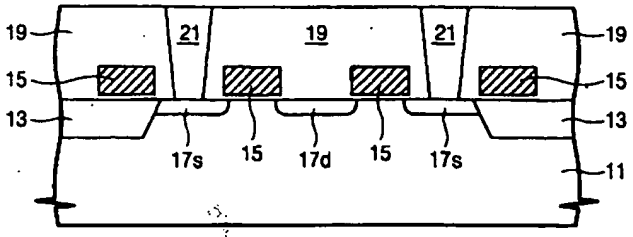

FIG. 2

(PRIOR ART)

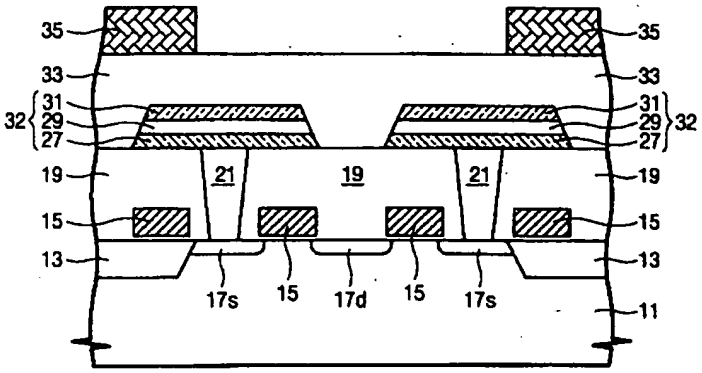

FIG. 3

(PRIOR ART)

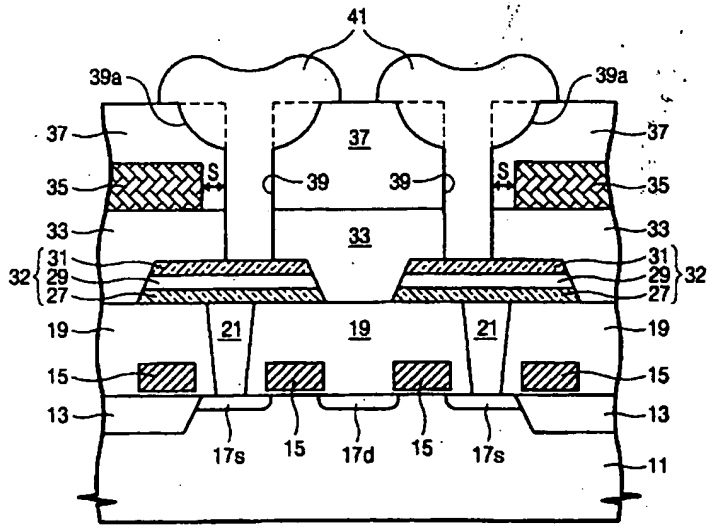

FIG. 4

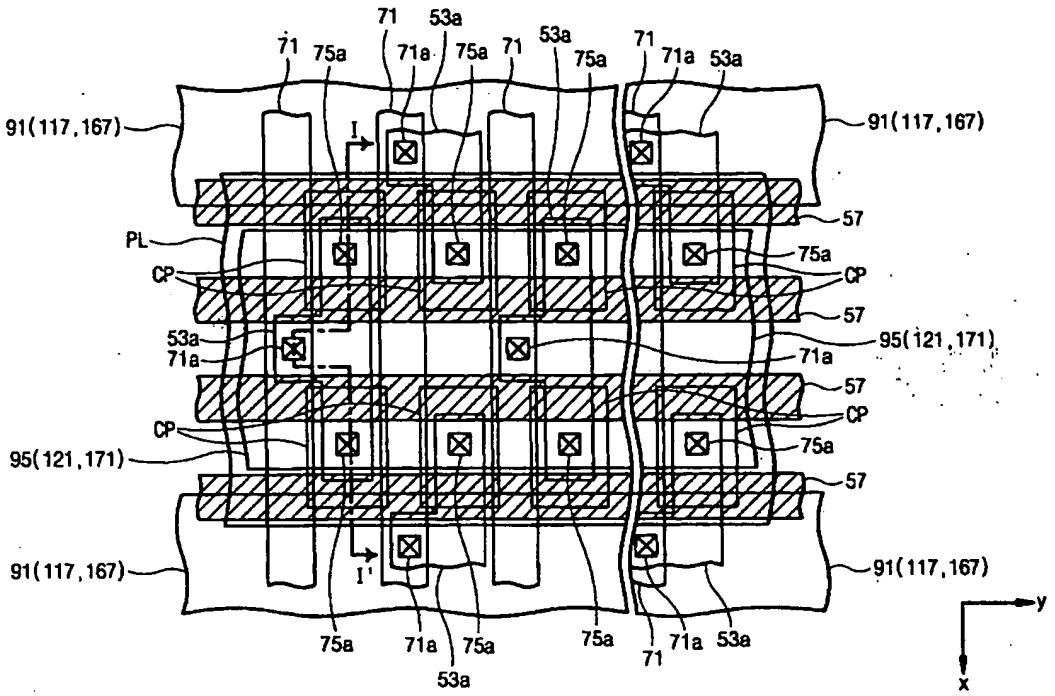

FIG. 5

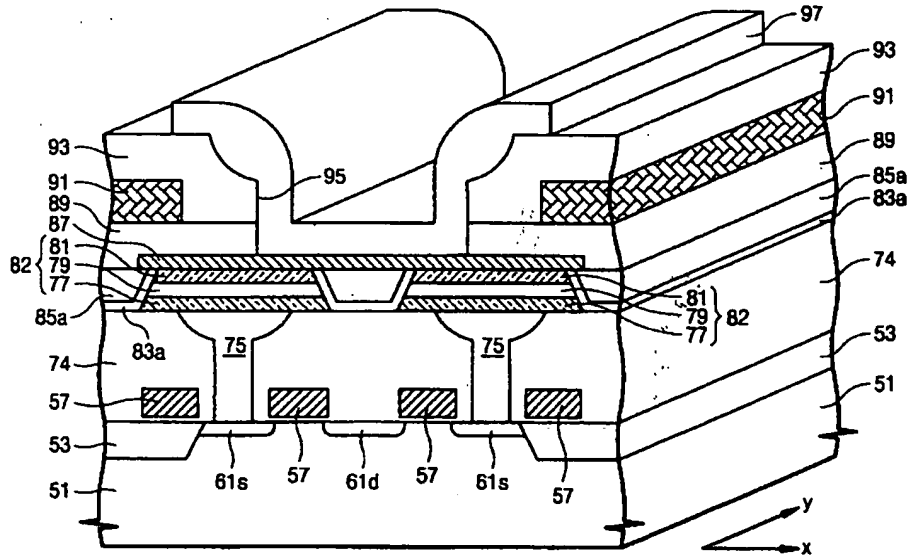

FIG. 6

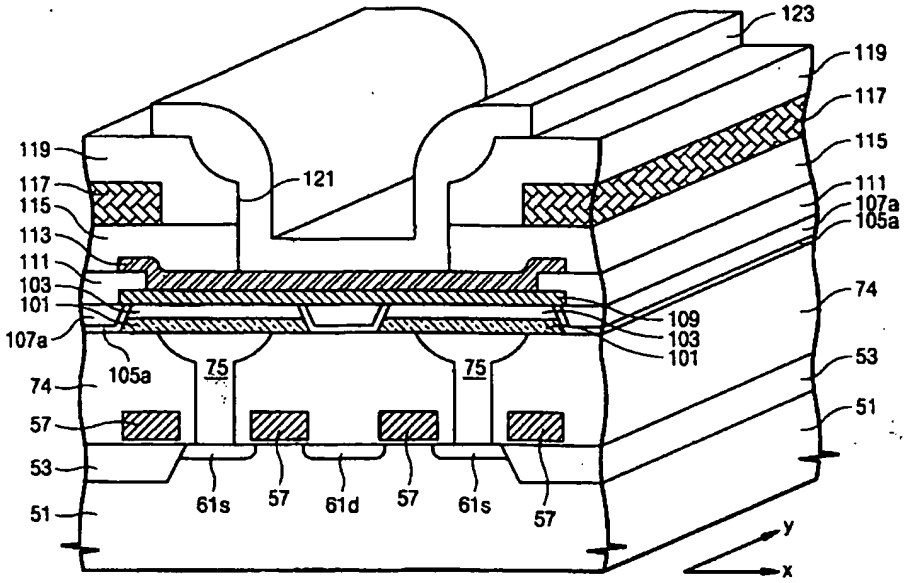
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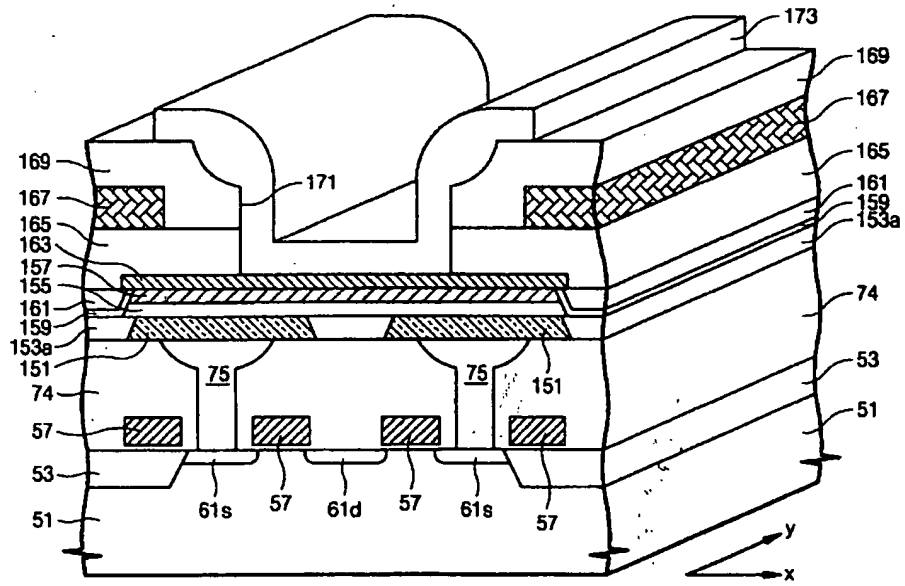
FIG. 7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x

FIG. 8

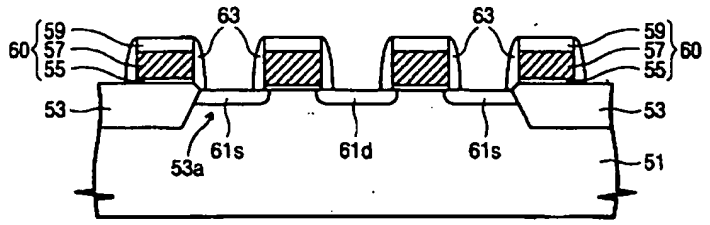

FIG. 9

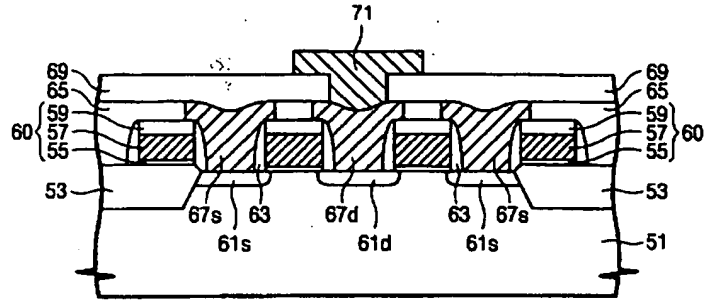

FIG. 10

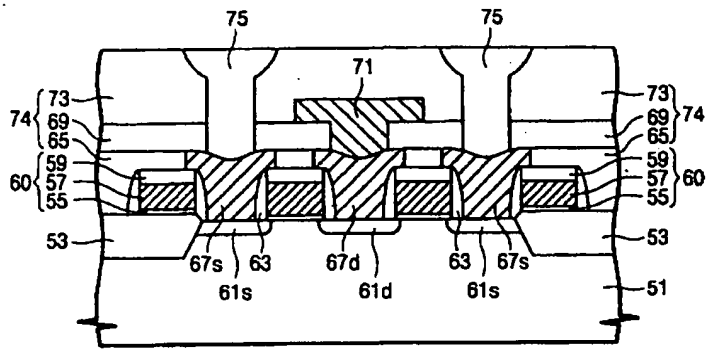

FIG. 11

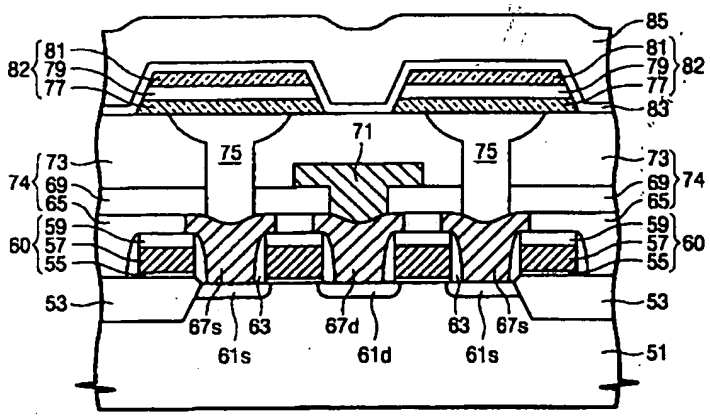

FIG. 12

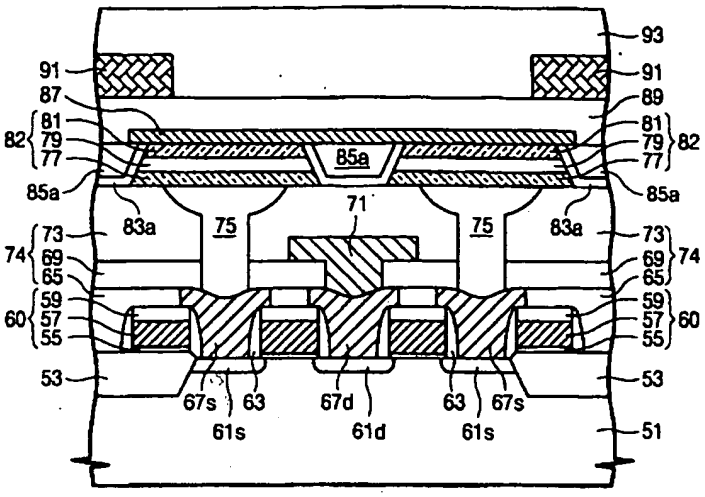
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FIG. 13

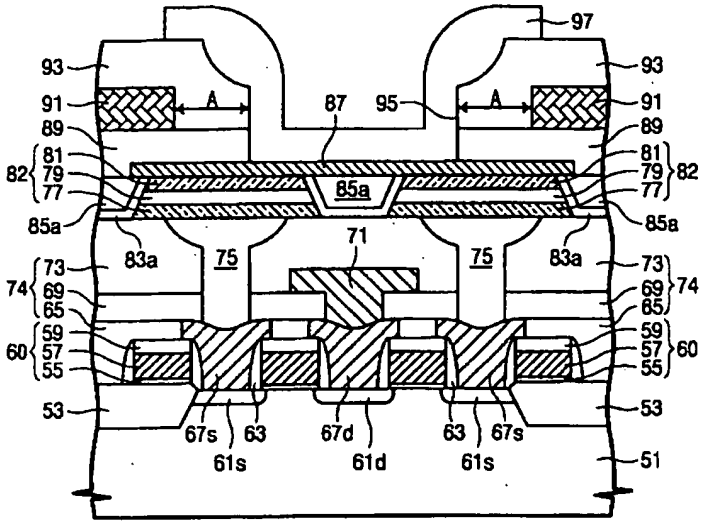
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FIG. 14

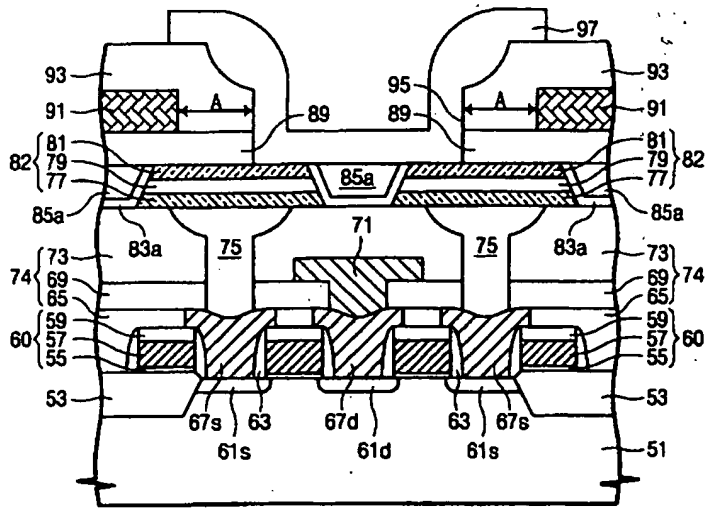
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FIG. 15

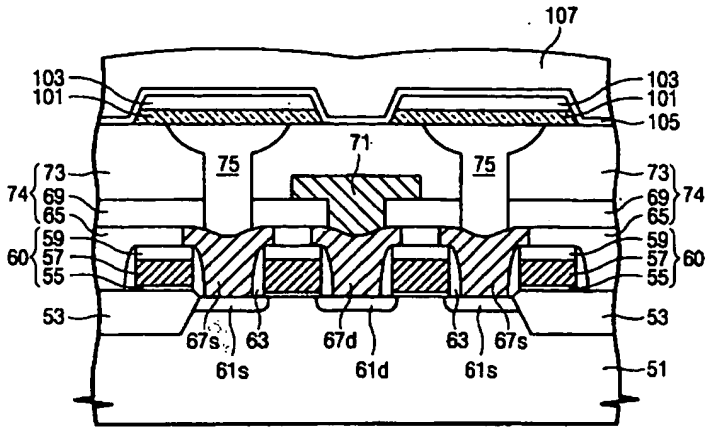

FIG. 16

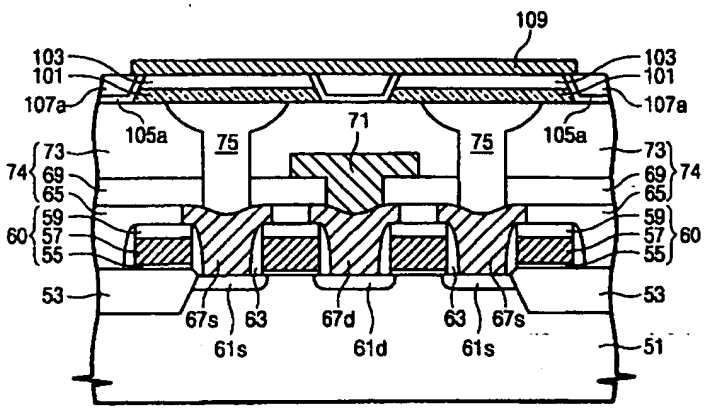

FIG. 17

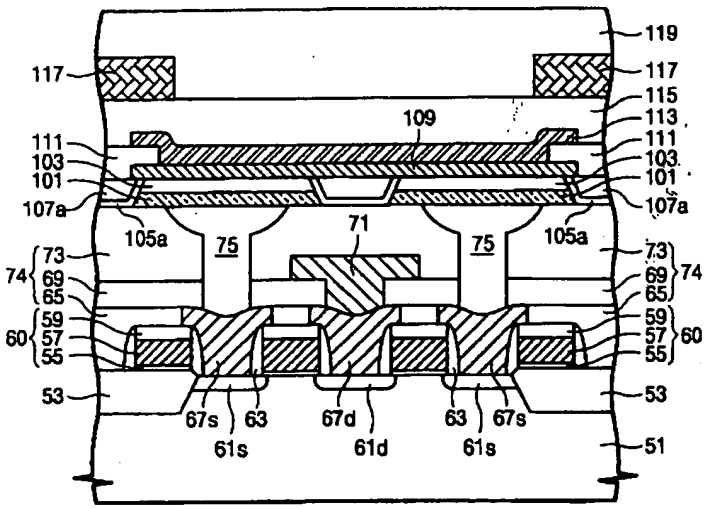

FIG. 18

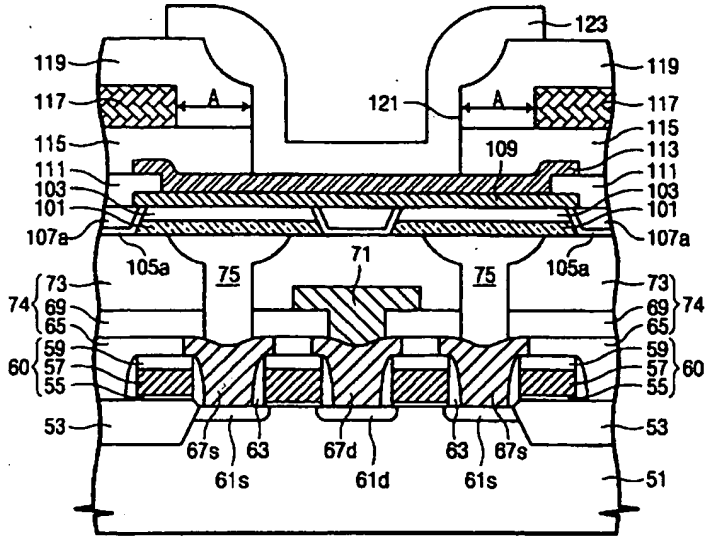

FIG. 19

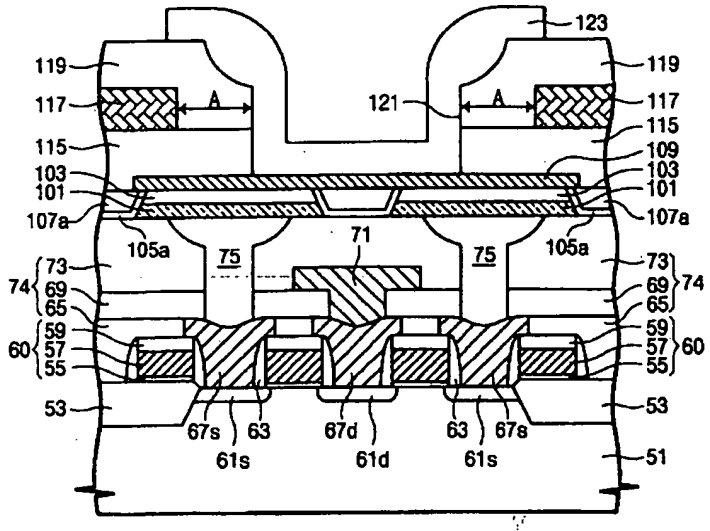

FIG. 20

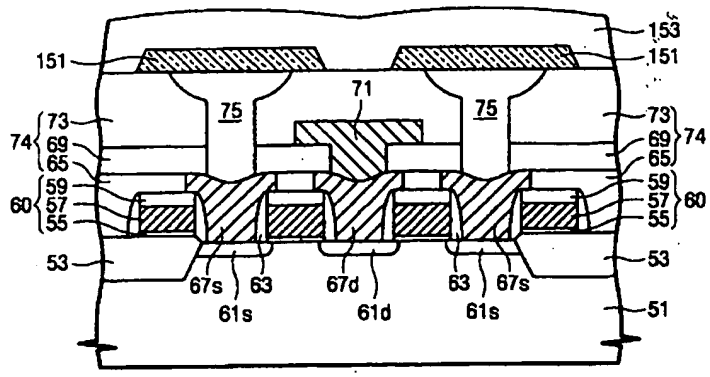

FIG. 21

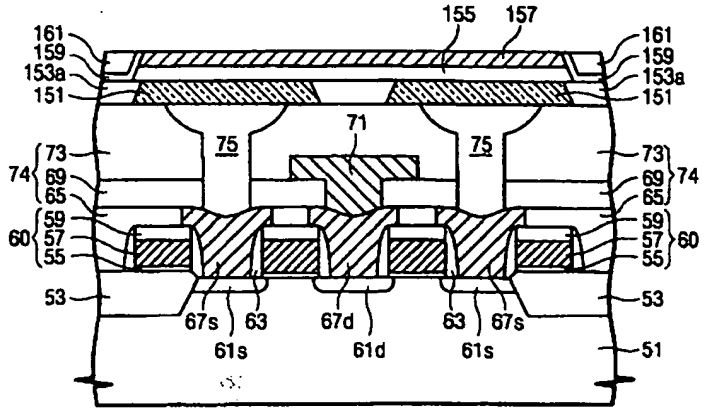

FIG. 22

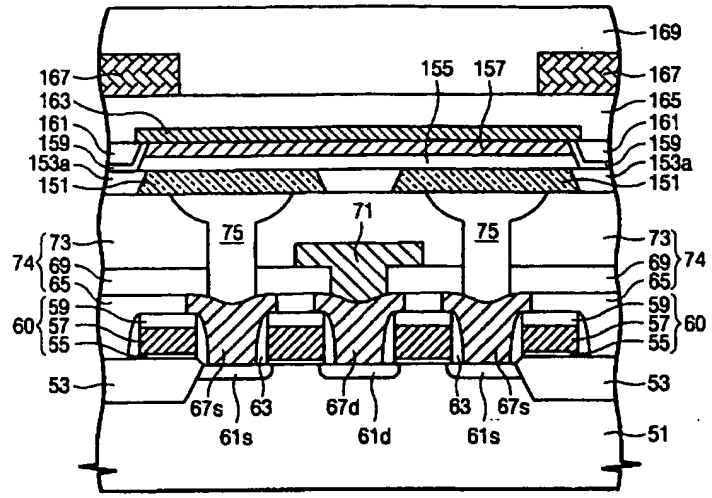

FIG. 23

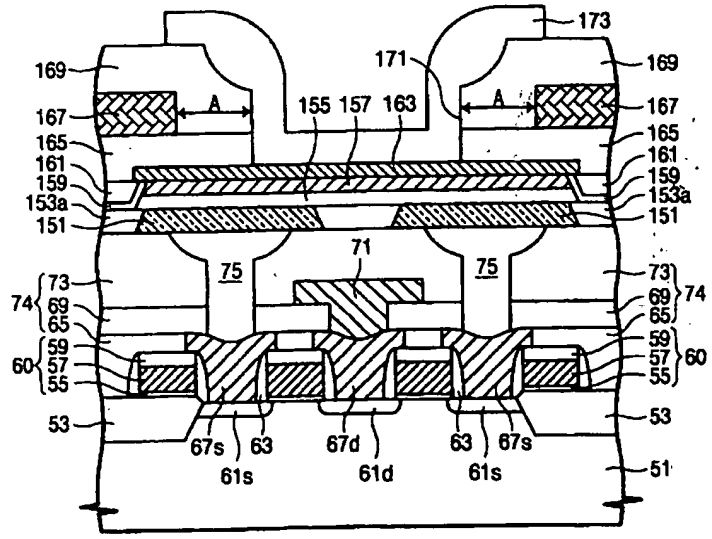

FIG. 24

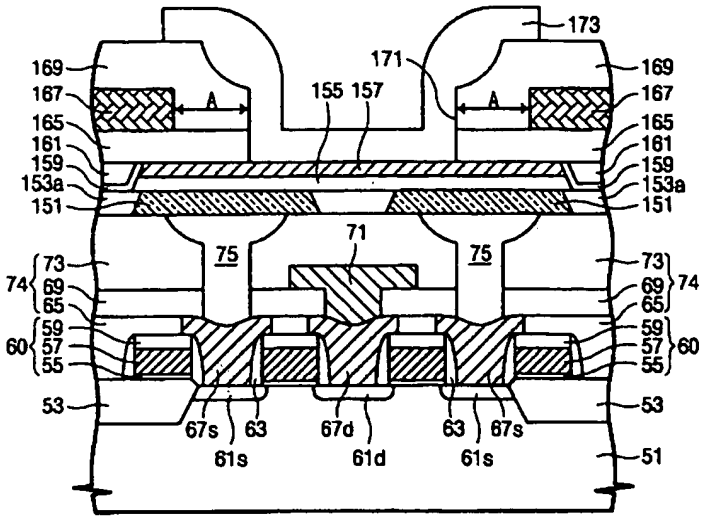
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FIG. 25

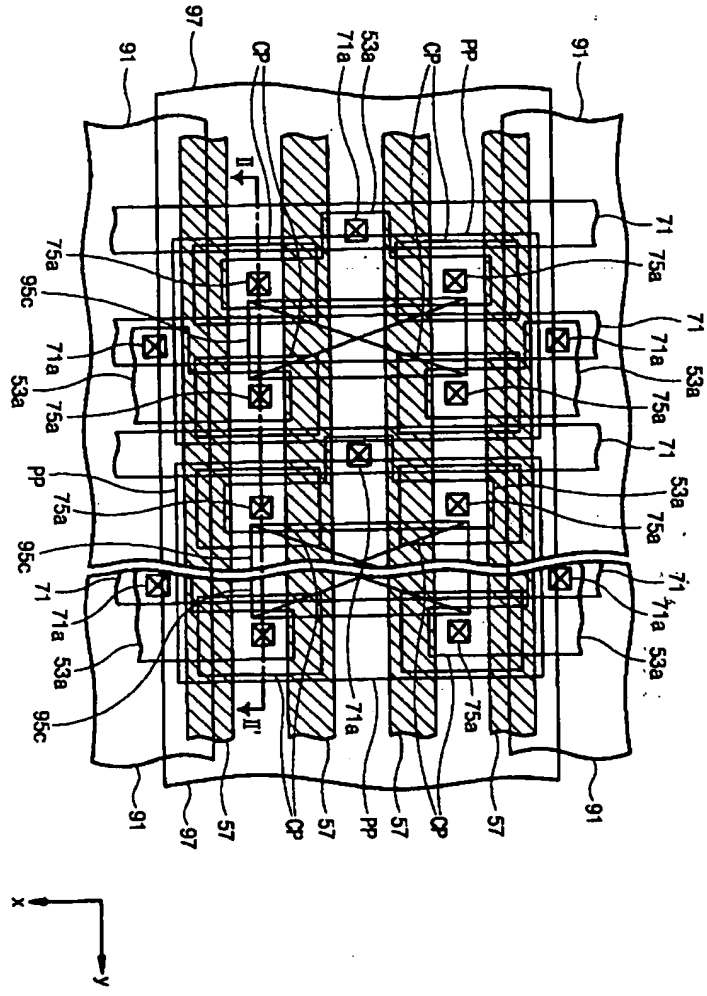
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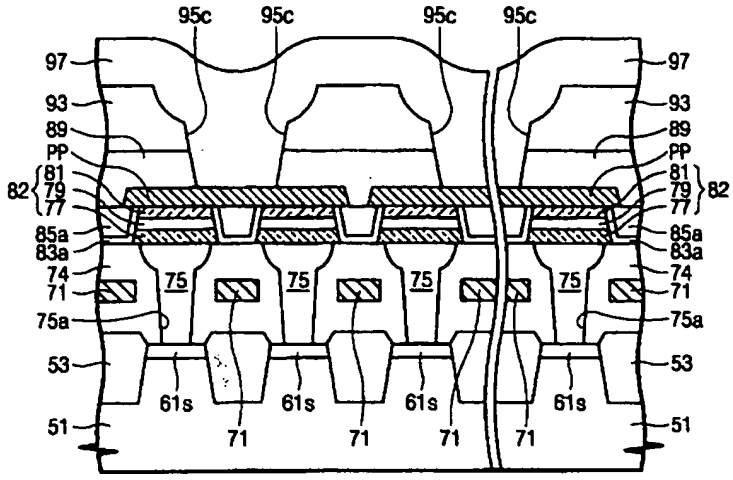
FIG. 26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